KPCI-PDISO8A and KPCI-PIO32IOA Specifications

These two products are to achieve a PCI version of the PDISO-8 and PIO32-IO ISA cards.

Control Inputs[1]

Quantity: 8 KPCI-PDISO8A
16 KPCI-PIO32IOA

Type: Solid-State, Opto-isolated

DC Inputs without optional filter

PARAMETER	MIN.	TYP.	MAX.	UNIT
Voltage Input Logic High	+/- 2.5		+/- 60	V_{DC}
Voltage Input Logic Low			+/- 1.0	V_{DC}
Response Time		0.6	1.0	ms
Isolation[2]	60			V pk

AC Inputs with optional filtering[3]

PARAMETER	MIN.	TYP.	MAX.	UNIT
Low Pass Filter Time Constant		175		ms
AC Sense Voltage Logic High	10		42	V pp
AC Sense Voltage Logic Low			< 10	V pp
AC Line Frequency Sensing		50 and 60		Hz

Interrupt Line Assignment

PARAMETER	Signal	Location	Pin #
External Interrupt Enable	INT_ENN	IP7	3,21
External Interrupt Request	INT_REQ	IP6	4,22

Outputs

Quantity: 8 KPCI-PDISO8A
16 KPCI-PIO32IOA

Type: Solid-State, Opto-isolated N.O. Relay (Form A)

AC/DC Load Switching

PARAMETER	MIN.	TYP.	MAX.	UNIT
Load Voltage				
DC			+/-60	V_{DC}
AC			30	V_{RMS}
Load Current[4]				
DC			350	mA $_{DC}$
AC			247	mA $_{RMS}$
Off State Leakage Current[5]		316	2000	nA
On State Channel Resistance [7]		3.5	4.0	Ω
Relay Turn ON Time		1.0	3.5	ms

PARAMETER	MIN.	TYP.	MAX.	UNIT
Relay Turn OFF Time		80	200	µs
Power Dissipation				
Per Channel			430	mW
Isolation [2]	60			V pk

NON-Isolated external power[6]

PARAMETER	Maxiumum Capacity	Location	Pin #
+5 V_{DC} PC Bus Sourced	1.0 Amperes	+5V	1 Top & Bot Connector
Digital Ground Return	1.0 Amperes	GND	19 Top & Bot Connector

GENERAL SPECIFICATIONS

POWER REQUIREMENTS: +5V: 500 mA Maximum

EMC: Conforms to European Union Directive 89/336/EEC, EN61326-1

SAFETY: Conforms to European Union Directive 73/23/EEC, EN61010-1

ENVIRONMENTAL:

Operating Temperature: 0 to 50°C

Storage Temperature: -20 to 70°C

Humidity (non condensing): 0 to 80% at 35°C

DIMENSION: 18.1cm x 10.8cm x 1.9cm (7.1in x 4.25in x 0.75in)

WEIGHT: KPCI-PIO32IOA – 0.13kg (0.30lbs) KPCI-PDISO8A – 0.12kg (0.26lbs)

ACCESSORIES:

Cables: CAB-1284CC-0.5, CAB-1284CC-2

STP-36: 36-pin Screw Terminal Panel

Notes:

1. Inputs are not guaranteed to be compatible with all TTL/CMOS logic families.
2. Minimum guaranteed isolation, which includes channel to channel, channel to PC and channel to chassis ground.
3. Selectable, jumper switched LPF. Recommended for AC or slow DC inputs.
4. De-rate 3.6 mA/°C if ambient temperature is over 25°C.
5. Output channel in off-state, T_A = 50°C, 60 V_{DC} applied with 30% RH (non-condensing) for maximum and typical values.
6. For convenience only. These are not isolated from the rest of the system. Do not use directly in external circuit if isolation is required.
7. Typical measurement was achieved with an STP-36 and 2 meter cable, CAB-1284CC-2 at 25°C.

Board Address Mapping

	Offset (byte)	Content	Description
BADDRx	0	Port A	Read Only – Input Register
	1	Port B	Read Only (KPCI-PIO32IOA Only)
	2	NA	
	3	Control	Latching control (R/W)
	4	Port A'	Readback / Write – Output Register
	5	Port B'	Readback / Write (KPCI-PIO32IOA Only)
	6	NA	
	7	NA	
	…		
	34 - 37	FW Rev	ASCII format: "A0xx" (Read Only)
	38 - 3A	INT CSR	Interrupt Control Register (R/W)
	3B	NA	

BADDRx + 0x03

Control Byte Format:

-- Bit 7 - This bit to be ignored.
-- Bit 6 - Access Mode Select – For B5 and B6 see table below.
-- Bit 5 - Access Mode Select – For B5 and B6 see table below.
-- Bit 4:0 - These bits to be ignored.

B6 B5 (Control byte)

0 0 – No input latching on rising interrupt edge.
0 1 – Latch group inputs on rising interrupt edge.
1 0 – No input latching on falling interrupt edge.
1 1 – Latch group inputs on falling interrupt edge.

BADDRx + 0x38

Interrupt Status Register Format: (DWord Access)
(Taken from the AMCC Architecture – used on KPCI-PIOs and KPCI-3160)
--**Bit 23** – Interrupt missed =1 for missed interrupt. Write 1 to acknowledge/clear.
--Bit 22:18 – These bits to be ignored.
--**Bit 17** – Interrupt pending = 1 for pending interrupt. Write 1 to acknowledge/clear.
--Bit 16 – This bit to be ignored.

--Bit 15:13 – These bits to be ignored.
--**Bit 12** – Interrupt enable = 1, HW Interrupts enabled, 0 = HW Interrupts disabled.
--Bit 11:08 – These bits to be ignored.

--Bit 7 – This bit to be ignored.
--**Bit 6** – Interrupt polarity select = 1 for falling edge, Write 0 for rising edge.
--Bit 5:0 – These bits to be ignored.

(x = 0 or 1) IO mapped use BADDR0. Memory mapped use BADDR1.

KPCI-PIO32IOA and KPCI-PDISO8A Pin Assignment

Top Connector

Pin #	Signal	Pin #	Signal
1	+5V	19	GND
2	-	20	-
3	IP7	21	IP7
4	IP6	22	IP6
5	IP5	23	IP5
6	IP4	24	IP4
7	IP3	25	IP3
8	IP2	26	IP2
9	IP1	27	IP1
10	IP0	28	IP0
11	OP7	29	OP7
12	OP6	30	OP6
13	OP5	31	OP5
14	OP4	32	OP4
15	OP3	33	OP3
16	OP2	34	OP2
17	OP1	35	OP1
18	OP0	36	OP0

Bottom Connector (For KPCI-PIO32IOA only)

Pin #	Signal	Pin #	Signal
1	+5V	19	GND
2	-	20	-
3	IP15	21	IP15
4	IP14	22	IP14
5	IP13	23	IP13
6	IP12	24	IP12
7	IP11	25	IP11
8	IP10	26	IP10
9	IP9	27	IP9
10	IP8	28	IP8
11	OP15	29	OP15
12	OP14	30	OP14
13	OP13	31	OP13
14	OP12	32	OP12
15	OP11	33	OP11
16	OP10	34	OP10
17	OP9	35	OP9
18	OP8	36	OP8